



Arm Cortex-R82AE Processor MP131

Software Developer Errata Notice

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Non-Confidential

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This document contains all known errata since the r0p0 release of the product.



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There might be a later issue at <http://developer.arm.com/documentation/SDEN-3362649>

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Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A (Rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B (Rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The [errata summary table](#) identifies errata that have been fixed in each product revision.

August 14, 2024: Changes in document version v2.0

ID	Status	Area	Category	Summary
3348876	New	Programmer	Category B	Precise ECC error in L1 D-cache tag RAM when using both MM and LLRAM ports might lead to data corruption
3612620	New	Programmer	Category B	CHI atomic load/cmp/swap with NDERR response and ACP read to same address can lead to deadlock
3619402	New	Programmer	Category B	Write requests occurring during online MBIST entry can cause data corruption
3625277	New	Programmer	Category B	Incorrect ECC code generation when writing to the L2 data RAM via online MBIST
3626735	New	Programmer	Category B	Incorrect identification or missed bus timeout errors on the LLPP interface
3267557	New	Programmer	Category C	ECC error in L1 D-cache tag RAM might not get logged in RAS record
3337316	New	Programmer	Category C	DCLS may lose lockstep under WARM_RESET
3355027	New	Programmer	Category C	PMC100_MER.FAE bit may not be appropriately set for the Cluster Online MBIST controller
3367453	New	Programmer	Category C	IMP_CLUSTERACTLR_EL1.L2SPEC specification is incorrect
3379590	New	Programmer	Category C	RTL forces latencies values different from the one expected while programming cluster PMC100_CFGR field
3384749	New	Programmer	Category C	Flop parity error before a Warm reset might corrupt the RAS error record
3471059	New	Programmer	Category C	Unused utility bus address locations are aliased
3581440	New	Programmer	Category C	PMC100_MER.FAE bit may not be appropriately set for the Core Online MBIST controller
3610023	New	Programmer	Category C	An external Non-cacheable store exclusive receiving a bus error response might not raise an asynchronous abort
3612655	New	Programmer	Category C	L2 Flushes too many ways when moving from FULL_RAM to HALF_RAM
3614585	New	Programmer	Category C	CHI DVM SNP Sync may lead to deadlock for Online MBIST entry
3622586	New	Programmer	Category C	In the presence of a hardware fault the Cluster ELA is able to impact functional execution performance of the processor
3640301	New	Programmer	Category C	Cold debug recovery reset will not reset some system registers

March 14, 2024: Changes in document version v1.0

No errata in this document version.

Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
3348876	Programmer	Category B	Precise ECC error in L1 D-cache tag RAM when using both MM and LLRAM ports might lead to data corruption	r0p0	Open
3612620	Programmer	Category B	CHI atomic load/cmp/swap with NDERR response and ACP read to same address can lead to deadlock	r0p0	Open
3619402	Programmer	Category B	Write requests occurring during online MBIST entry can cause data corruption	r0p0	Open
3625277	Programmer	Category B	Incorrect ECC code generation when writing to the L2 data RAM via online MBIST	r0p0	Open
3626735	Programmer	Category B	Incorrect identification or missed bus timeout errors on the LLPP interface	r0p0	Open
3267557	Programmer	Category C	ECC error in L1 D-cache tag RAM might not get logged in RAS record	r0p0	Open
3337316	Programmer	Category C	DCLS may lose lockstep under WARM_RESET	r0p0	Open
3355027	Programmer	Category C	PMC100_MER.FAE bit may not be appropriately set for the Cluster Online MBIST controller	r0p0	Open
3367453	Programmer	Category C	IMP_CLUSTERACTLR_EL1.L2SPEC specification is incorrect	r0p0	Open
3379590	Programmer	Category C	RTL forces latencies values different from the one expected while programming cluster PMC100_CFGR field	r0p0	Open
3384749	Programmer	Category C	Flop parity error before a Warm reset might corrupt the RAS error record	r0p0	Open
3471059	Programmer	Category C	Unused utility bus address locations are aliased	r0p0	Open
3581440	Programmer	Category C	PMC100_MER.FAE bit may not be appropriately set for the Core Online MBIST controller	r0p0	Open

ID	Area	Category	Summary	Found in versions	Fixed in version
3610023	Programmer	Category C	An external Non-cacheable store exclusive receiving a bus error response might not raise an asynchronous abort	r0p0	Open
3612655	Programmer	Category C	L2 Flushes too many ways when moving from FULL_RAM to HALF_RAM	r0p0	Open
3614585	Programmer	Category C	CHI DVM SNP Sync may lead to deadlock for Online MBIST entry	r0p0	Open
3622586	Programmer	Category C	In the presence of a hardware fault the Cluster ELA is able to impact functional execution performance of the processor	r0p0	Open
3640301	Programmer	Category C	Cold debug recovery reset will not reset some system registers	r0p0	Open

Errata descriptions

Category A

There are no errata in this category.

Category A (rare)

There are no errata in this category.

Category B

3348876

Precise ECC error in L1 D-cache tag RAM when using both MM and LLRAM ports might lead to data corruption

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category B

Fault Status: Present in r0p0. Open

Description

The L1 data cache tag RAM provides SEDDED protection against errors, because of this erratum when an error occurs in specific bits of the L1 data cache tag RAM it might results in data corruption from some cache states.

Configurations affected

This erratum affects configurations of the Cortex-R82AE processor where the *Low-latency RAM* (LLRAM) port is implemented (**LLRAM** configuration parameter is set to 1).

Conditions

This erratum occurs when the following sequence of conditions are met:

1. Cachelines for the *Main Manager* (MM) port are stored in the L1 data cache
2. A cache lookup for a load instruction occurs for an LLRAM address which is not in the cache
3. An error occurs in the L1 data cache tag RAM which appears to change the state of a MM cacheline from valid to invalid
4. The linefill for the LLRAM lookup does not allocate into the cache
5. Another cache lookup for a load instruction is performed for the same LLRAM cacheline
6. Additional micro-architectural conditions occur

Implications

When this erratum occurs, the linefill for the second cache lookup overwrites a valid cacheline for the MM port. This might cause silent data corruption. The error is not reported to RAS, but would be reported if a MM cache lookup was performed for the same set.

Workaround

In order to work around this erratum, set IMP_CPUACTLR_EL1.DCWT (bit 36) to 0. This might have a small power impact on some workloads.

Because this erratum occurs when there is an ECC error and because the ECC errors are not expected in sample silicon, it is still practical to evaluate the performance with IMP_CPUACTLR_EL1.DCWT=1 for sample silicon.

3612620

CHI atomic load/cmp/swap with NDERR response and ACP read to same address can lead to deadlock

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category B

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor can optionally send coherent atomic requests externally on the CHI interface when broadcastatomic is set. Due to this erratum, L2 can deadlock from a CPU coherent load/compare/swap atomic never releasing an address hazard.

Configurations affected

This erratum affects configurations of the Cortex-R82AE processor which include a main manager CHI interface with broadcastatomics set.

Conditions

This erratum occurs when all of the following conditions are met:

- A core makes a coherent load, compare or swap atomic that goes out externally on the CHI interface
- The cluster holds a copy of the cache line addressed by the atomic
- The CHI interface returns an NDERR response without performing a snoop based on the TXREQ snoopme bit
- An ACP coherent read request to the same address as the atomic hits in the cluster

Implications

If this erratum occurs then the cluster can maintain an indefinite address hazard on the address used by the CPU coherent atomic. The CPU core will get an NDERR response forwarded to it, but the ACP read request will never complete. A deadlock can occur in the L2 due to the persistent hazarding blocking forward progress of other traffic. The CPU core will take an abort based on the NDERR response it receives.

This is not expected to impact most systems due to getting an NDERR response in combination with timing of an ACP read request to the same location being rare. For interrupt latency it is recommended to force all atomics near which would prevent this erratum from occurring. It is not expected that Cortex-R82AE will be used in large systems so forcing atomics near should have minimal performance impact.

Workaround

Force atomics near by setting either IMP_CPUACTLR_EL1.ATOM to 0b01 or broadcastatomic = 0.

3619402

Write requests occurring during online MBIST entry can cause data corruption

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category B

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor supports online MBIST access to the L2 data buffer RAMs. A request to enter into online MBIST will allow outstanding requests to complete whilst blocking any new requests from starting. Once the outstanding requests have completed online MBIST can then have sole access to the RAMs. Data corruption can occur if there are new write requests being made by the cores when there is an online MBIST request to access the L2 data buffer RAMs. This occurs because there exists a small window where a new write request is allowed to proceed when an online MBIST access is made resulting in potential corruption of L2 data buffer RAM.

Configurations affected

This erratum affects all configurations of the Cortex-R82AE processor where online MBIST is used.

Conditions

This erratum occurs when all of the following conditions are met:

- Online MBIST entry request to access the L2 data buffer RAMs
- Timing conditions to hit a 1-cycle window
- A core write request that doesn't perform its L2 data buffer RAM access before online MBIST performs an access

Implications

Online MBIST could perform L2 data buffer RAM accesses that could lead to data corresponding to the new write request being lost and hence lead to data corruption. Hitting the 1-cycle window is difficult and in part relies on the Core delaying the draining of write data which is rare.

Workaround

There is no workaround for this issue. Therefore it is recommended not to use this function, except for engineering samples to develop test software.

3625277

Incorrect ECC code generation when writing to the L2 data RAM via online MBIST

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category B

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor supports an address folding feature where some or all of a RAM address are factored into the ECC code to protect against address encoding and decoding errors. Online MBIST has a feature that allows writes to the RAMs where the functional path in the Cortex-R82AE processor can be selected to generate the appropriate ECC code to match the data that is being written to a RAM location by MBIST. This erratum relates to an issue where the wrong ECC code is generated by the Cortex-R82AE processor when performing a write to the L2 data RAM. This can result in errors when using online MBIST to test the ECC logic in the Cortex-R82AE processor.

Configurations affected:

This erratum uniquely affects a Cortex-R82AE processor configured with Online MBIST and an L2 cache size larger than zero.

Conditions:

This erratum occurs when the following sequence of conditions is met:

- Online MBIST writes to the L2 data RAM where the Cortex-R82AE ECC generation logic is selected to create an ECC code
- The value on the two address ports from the MBIST controller are not the same

Typically dual ported RAMs have one address port for reads and another address port for writes. The L2 data RAM is a single port RAM and therefore one address port is used for both reads and writes. However, the second address output from the MBIST controller was being used to generate the ECC code for the L2 data RAM and an incorrect ECC code can be generated if this second address output doesn't match the first address output.

Implications:

False errors are generated by MBIST checks on the ECC generation logic and therefore a customer should avoid such tests and only access the RAMs in direct mode and bypass the ECC generation logic.

Workaround:

This issue can be mitigated if the two address outputs from the MBIST controller have matching values when writing data to the L2 data RAM via online MBIST when selecting to go through the ECC generation logic. If the Arm PMC-100 Programmable MBIST Controller is used this can be achieved by programming the BAMEN register to 1'b1.

3626735

Incorrect identification or missed bus timeout errors on the LLPP interface

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category B

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor supports a bus timeout feature on the *Low Latency Peripheral Port* (LLPP) to trigger an error when the bus has not been responsive in a set period of time. This erratum relates to an issue where a false bus timeout error may be generated when there are no requests outstanding on the LLPP interface. In rare circumstances, this erratum could lead to a scenario where a bus timeout error isn't generated when one should have been generated.

Configurations affected:

This erratum uniquely affects a Cortex-R82AE processor configured with bus timeout on systems that utilise the LLPP which is clocked at a rate that is slower than the CPU by toggling the ACLKEN signal.

Conditions:

This erratum occurs when the following sequence of conditions is met:

- Bus timeout is enabled via setting IMP_BUSTIMEOUTR_EL1.ENABLELLPP
- The LLPP interface is configured with a $N > 1$ for an N:1 clock ratio by toggling the ACLKEN signal
- The CPU is speculatively executing a load which is targeting the LLPP port which is interrupted before it is architecturally executed

Implications:

When this erratum occurs, false LLPP bus timeout errors can be generated and may lead to unexpected triggering of fault handlers. In rare cases this erratum can lead to a bus timeout error not being triggered on the LLPP interface for a real bus timeout issue which could result in a system deadlock if an LLPP request never returns a response. In the case a bus timeout error is not triggered when it should have been then a system watchdog may generate an interrupt, but the cause of the deadlock may be unknown.

Workaround:

In order to workaround this erratum implement an LLPP interface with a 1:1 clock ratio or don't use bus timeout on the LLPP interface.

Category B (rare)

There are no errata in this category.

Category C

3267557

ECC error in L1 D-cache tag RAM might not get logged in RAS record

Status

Affects: Cortex-R82AE
Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor supports reporting errors via the *Reliability, Availability, and Serviceability* (RAS) registers. Due to this erratum, it is possible that a corrected error in the L1 data cache Tag RAM is not reported.

Configurations affected

This erratum affects all configurations of the Cortex-R82AE processor.

Conditions

This erratum occurs when the following sequence of conditions is met:

1. An error has previously occurred in the L1 data cache, in either the data RAM or the tag RAM
2. A cacheline containing data for the *Low-latency RAM* (LLRAM) port is held in the L1 data cache
3. A linefill is performed for a *Main Manager* (MM) address, for example due to a load or store instruction or a pagewalk, which uses the same set and way as the LLRAM cacheline
4. A cache lookup occurs to the same set as the previous error, for example due to a load or store instruction or a pagewalk
5. An new error occurs in the L1 data cache tag RAM for the set and way of the linefill that was started for the MM address in condition 3, with no other cache lookups being performed

Implications

When this erratum occurs, the Tag RAM contents will be updated with the correct data for the new cacheline, but the correction of the error will not be reported in the RAS registers.

There is still significant benefit gained from the ECC logic because this erratum does not impact the correction of the ECC errors affected. It only affects the reporting of the corrected errors in the error record registers.

Workaround

No workaround is required for this erratum.

3337316

DCLS may lose lockstep under WARM_RESET

Status

Affects: Cortex-R82AE
Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor can be configured to support core-level redundancy and lockstep comparators. As a result of this erratum, the redundant cores may lose lock step with the primary cores if external debug accesses are performed at the same time as a power transition to or from the WARM_RESET or EMU_OFF states.

Configurations affected

Configurations of Cortex-R82AE configured to support LOCK or HYBRID_LOCK are affected.

Conditions

The erratum occurs when all of the following conditions are true:

- The processor is operating in LOCK mode
- A debug access to core registers is performed
- A power transition to or from WARM_RESET or EMU_OFF is performed at the same time

Implications

When the processor is operating in a mission mode safety critical scenario, any debug access will trigger an inadvertent activation fault. Debug accesses and use of the WARM_RST state or EMU_OFF state is not expected in mission mode.

The primary debug access will complete as expected but depending in micro-architectural timing conditions there may be a loss of synchronisation between the primary and redundant processors. There may also be a loss of synchronisation between the primary and redundant clusters which will be reported through one of the DCLSFAULT output pins. Under some timing conditions, the DCLSFAULT report may affect just the redundant cluster checkers.

Workaround

There is no workaround.

3355027

PMC100_MER.FAE bit may not be appropriately set for the Cluster Online MBIST controller

Status

Affects: Cortex-R82AE
Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor can optionally implement a PMC100 MBIST controller, which provides *Online MBIST* (OLMBIST) functionality to the cluster. Due to this erratum, if the L2 unit receives functional traffic from subordinates whilst in OLMBIST mode, the L2 will not raise the PMC100_MER.FAE bit as expected. This is intended to indicate a software error has occurred, when the L2 has received coherent requests which target the L2 TAG or L2 Data RAMs.

Configurations affected

This erratum affects configurations of the Cortex-R82AE processor which include the PMC100 OLMBIST Controller (PMC = 1).

Conditions

This erratum occurs if the L2 receives coherent requests targeting the L2 Tag or L2 Data RAM under test, whilst performing Online MBIST testing in *Offline Memory Use Model*. The *Online Memory Use Model* is not affected.

Note that in the *Offline Memory Use Model* it is assumed the memory to be tested is disabled via software and is not available for functional use. This assumption must be violated for this erratum to occur.

Implications

If this erratum occurs, coherency may be lost within the L2 without any indication to software that this has occurred, because the PMC100_MER.FAE error flag is not raised.

Workaround

If the Offline Memory Use Model is required for Online MBIST, software should not rely on the status of PMC100_MER.FAE bit to indicate functional access has occurred during Online MBIST.

3367453

IMP_CLUSTERACTLR_EL1.L2SPEC specification is incorrect

Status

Affects: Cortex-R82AE
Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open

Description

The IMP_CLUSTERACTLR_EL1.L2SPEC register bit which is documented as controlling L2 cache speculative accesses can be read and written, but has no effect on the processor

Configurations affected

The erratum affects all configurations of the Cortex-R82AE processor.

Conditions

This erratum occurs when the following condition takes place:

- The IMP_CLUSTERACTLR_EL1.L2SPEC register is written with a non-zero value

Implications

L2 cache speculative accesses are still enabled.

Workaround

IMP_CLUSTERACTLR_EL1.L2SPEC should be written as zero.

3379590

RTL forces latencies values different from the one expected while programming cluster PMC100_CFGR field

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category C

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE process can optionally implement a PMC100 MBIST controller, which provides *Online MBIST* (OLMBIST) functionality to the cluster. Because of this erratum, when performing OLMBIST to the L2 Data memories, the memory latencies that are used are different to the ones programmed in the PMC100_CFGR.

Configurations affected

This erratum affects all configuration with PMC100 enabled and L2 Cache is present:

- The PMC configuration parameter is set to 1
- The **L2_CACHE_SIZE** configuration parameter is set to a value greater than 0

Conditions

1. OLMBIST test ongoing for L2DATA rams
2. L2DATA latencies are different from the minimum or maximum latencies

Implications

The programmed PMC100_CFGR latencies will be ignored and either the minimum or the maximum latencies will be applied. If the L2 Data memories cannot operate at either the minimum or the maximum latencies, the PMC100 tests will indicate false failures.

Workaround

In order to work around this erratum, program the PMC-100 to run at the slowest configuration for for L2DATA RAM testing by setting the following values:

- PMC100_CFGR = 5'b11010
- PMC100_MCR.RCOW = 3
- PMC100_MCR.RCOR = 3

- If L2_DATA_RD_SLICE == 0:
 - PMC100_MCR.PDP = 5
 - PMC100_MCR.PD = 5
- If L2_DATA_RD_SLICE == 1:
 - PMC100_MCR.PDP = 6
 - PMC100_MCR.PD = 6

3384749

Flop parity error before a Warm reset might corrupt the RAS error record

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category C

Fault Status: Present in rOp0. Open

Description

The Cortex-R82AE processor implements the *Reliability, Availability, and Serviceability* (RAS) Extension as defined in the Arm architecture. The Cortex-R82AE processor also implements transient fault protection.

Because of this erratum, a flop parity error which occurred right before a Warm reset might cause an invalid error recorded in the RAS registers.

Configurations affected

This erratum affects all configurations of the Cortex-R82AE processor.

Conditions

This erratum occurs when all the following conditions are met:

- The RAS error reporting and logging are enabled (`ERR7CTLR.ED == 1`)
- The transient fault protection reporting and logging are enabled (`IMP_MEMPROTCTLR_EL1.TFPEN == 1`)
- A Warm reset is asserted
- A transient fault is detected

Implications

There is still substantial benefit being gained from the ECC logic. There might be a negligible increase in overall system failure rate due to this erratum.

If this erratum occurs, RAS error record 7 will record an invalid error with none of fields `ERR7STATUS`. {CE,DE,UE} set. There will be no Error Recovery Interrupt or Fault Handling Interrupt asserted.

Workaround

No workaround is expected to be required. If an invalid RAS error record 7 is found after a Warm reset, a transient fault is deemed to have occurred.

3471059

Unused utility bus address locations are aliased

Status

Affects: Cortex-R82AE
Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open

Description

This erratum affects the default sparse address map mode. If a utility bus access is performed to an address in an unused 4kB address region, the access should be treated as RAZ/WI. Instead, the the access will be aliased onto an existing register location.

Configurations affected

This erratum affects the configuration with sparse address map (`DENSE_CS_ADDR_MAP = 0`).

Conditions

This erratum occurs when all the following conditions are met:

- A utility bus access is performed with non-zero offset address in the bit position 15 to 12.

Implications

If this erratum occurs, some external registers may be read or modified unintentionally. The register access restrictions for the alias locations are respected.

Workaround

No workaround is required.

3581440

PMC100_MER.FAE bit may not be appropriately set for the Core Online MBIST controller

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category C

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor can optionally implement a PMC100 MBIST controller, which provides *Online MBIST* (OLMBIST) functionality to the core. Due to this erratum, the L1 data cache might raise the PMC100_MER.FAE bit when the unit has not received functional traffic that would impact the OLMBIST testing. This is intended to indicate a software error has occurred, when the cache has received coherent requests which target the L1 Data Cache RAMs.

Configurations affected

This erratum affects configurations of the Cortex-R82AE processor which include the PMC100 OLMBIST Controller (PMC = 1).

Conditions

This erratum occurs if the core performed speculative accesses to the L1 Data Cache RAM under test or is in a low power state due to execution of a WFx instruction, whilst performing Online MBIST testing in *Offline Memory Use Model*. The *Online Memory Use Model* is not affected.

Note that in the *Offline Memory Use Model* it is assumed the memory to be tested is disabled via software and is not available for functional use.

Implications

If this erratum occurs the PMC100_MER.FAE error flag is raised, although there was no functional access to the L1 Data Cache.

Workaround

If the Offline Memory Use Model is required for Online MBIST, software should not rely on the status of PMC100_MER.FAE bit to indicate functional access has occurred during Online MBIST.

3610023

An external Non-cacheable store exclusive receiving a bus error response might not raise an asynchronous abort

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category C

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor supports sending Non-cacheable or Device exclusives on the *Main Manager* (MM) and *Low-Latency RAM* (LLRAM) ports. If a Non-cacheable or Device store exclusive gets an error response, the store exclusive might only abort synchronously when it cannot be guaranteed that memory has not been updated.

Configurations affected

This erratum affects all configurations of the Cortex-R82AE processor.

Conditions

This erratum occurs when the following sequence of conditions is met:

1. An store exclusive instruction is executed with Non-cacheable or Device attributes
2. The store exclusive is sent on the MM or LLRAM port
3. The response to the store exclusive is an error response
 - For AXI, BRESP has a value of SLVERR or DECERR
 - For CHI, the response is a DErr or NDErr response
4. The memory targeted by the store exclusive is still modified despite the previous error occurring

Implications

If this erratum occurs a synchronous exception will be raised despite the associated memory location having been updated.

Workaround

No workaround is expected to be needed as it is expected that for most systems Non-cacheable and Device exclusives are not used, also this erratum can only occur when there is a bus error which might not be possible to recover from.

3612655

L2 Flushes too many ways when moving from FULL_RAM to HALF_RAM

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category C

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor supports the power down of half of the L2 cache in order to save power. Maintaining coherency and data consistency is achieved by evicting half of the data from the L2 cache before powering off the respective half of the L2 cache RAM. Due to this erratum, all the lines in the L2 cache are evicted rather than only the lines that are needed.

Configurations affected

This erratum affects configurations of the Cortex-R82AE processor where the L2 cache size is greater than zero.

Conditions

A power transition occurs from FULL_RAM to HALF_RAM operating mode.

Implications

All lines in the L2 cache are flushed rather than just the cachelines for the half of the cache being powered down. This can result in a performance loss due to the need to refetch some cache lines from main memory after the power mode transition.

Workaround

There is no workaround.

3614585

CHI DVM SNP Sync may lead to deadlock for Online MBIST entry

Status

Affects: Cortex-R82AE
Fault Type: Programmer Category C
Fault Status: Present in r0p0. Open

Description

If the CHI interface receives a DVM Sync on the snoop interface that is ongoing at the point when online MBIST is being entered then in some cases Cortex-R82-AE can deadlock.

Configurations affected:

This erratum uniquely affects a Cortex-R82AE processor configured with Online MBIST and a CHI manager interface

Conditions:

This erratum occurs when the following sequence of conditions is met:

- broadcastdvm = '1'
- A Snoop DVM sync as a result of a DVM sync from another RN-F
- Online MBIST entry request to an L2 RAM
- One or more CPUs with requests outstanding but blocked due to online MBIST entry
- Specific timing conditions met

Implications:

When this erratum occurs, the online MBIST entry will not complete and will result in system deadlock.

Workaround:

No workaround available for this erratum. No customer is expected to use this prior to REL.

3622586

In the presence of a hardware fault the Cluster ELA is able to impact functional execution performance of the processor

Status

Affects: Cortex-R82AE

Fault Type: Programmer Category C

Fault Status: Present in r0p0. Open

Description

The Cortex-R82AE processor is intended for use in safety critical applications with up to ISO26262 ASIL-D or IEC 61508 SIL-3 safety requirements. As part of the safety package it is assumed that debug logic will not be active during safe operation, and the Cortex-R82AE processor guarantees that random hardware faults within the debug logic do not affect the safe operation of the processor. Due to this erratum, a random hardware fault in the Cluster Embedded Logic Analyser is able to propagate to the interface and affect the function of the Cortex-R82AE processor.

Configurations affected

This erratum affects configurations of Cortex-R82AE that support at least DCLS Hybrid mode (CIMODE > 0) and have a Cluster ELA included (ELA=1).

Conditions

The erratum occurs when all of the following conditions are true:

- ELA is not enabled via debug block
- A random hardware fault in the Cluster ELA causes the CTTRIGOUT output to be asserted

Implications

When CTTRIGOUT is asserted packets will be sent on the internal AXI-Stream network responsible for routing internal and external register read/write packets and interrupts. This may increase the latency and reduce the throughput of non-debug packets, and may impact the safety case of the Cortex-R82AE processor - particularly for exceptions and system register accesses. The occurrence of this fault is not flagged by Cortex-R82AE's error detection mechanism.

Workaround

There is no workaround.

3640301

Cold debug recovery reset will not reset some system registers

Status

Affects: Cortex-R82AE

Fault type: Programmer Category C

Fault status: Present in r0p0. Open

Description

When a cold debug recovery reset is applied to the Cortex-R82AE processor system, there are some system registers that will not be reset to their initial value.

Configurations affected

The erratum affects any configurations of the Cortex-R82AE processor.

Conditions

This erratum can occur when the following sequence of events occurs:

1. Cluster power transition from OFF or MEM_RET to ON
2. CLUSTERPPU_PTCR.DBG_RECOV_PORST_EN has been programmed to be 1'b1
3. Cluster power transition from ON to DBG_RECOV
4. Cluster power transition from DBG_RECOV back to ON

Implications

When any cold debug recovery reset is applied, the following system register fields will not be reset to their corresponding initial value.

- IMP_CLUSTERACTLR_EL1.UBACCLVL
- IMP_CLUSTERACELSTLR_EL1.LLRAMACCLVL
- IMP_CLUSTERACELSTLR_EL1.TCMACCLVL<n>, where n is from 0 to NUM_CORES - 1
- IMP_CLUSTERPWRCTLR_EL1.PRTNRQ
- IMP_CLUSTERPWRDN_EL1.MEM_RET

Workaround

Arm does not expect a workaround to be required for this erratum.

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Product and document information

Read the information in these sections to understand the release status of the product and documentation, and the conventions used in the Arm documents.

Product status

All products and Services provided by Arm require deliverables to be prepared and made available at different levels of completeness. The information in this document indicates the appropriate level of completeness for the associated deliverables.

Product completeness status

The information in this document is Final, that is for a developed product.

Product revision status

The rxpy identifier indicates the revision status of the product described in this manual, where:

rx

Identifies the major revision of the product.

py

Identifies the minor revision or modification status of the product.